Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.092”**

**PAD FUNCTION:**

1. **–IN**
2. **+IN**
3. **OFFSET ADJ**
4. **OFFSET ADJ**
5. **V-**
6. **SIG. GND**
7. **OUTPUT**
8. **INT BANDWIDTH**
9. **V+**
10. **NC**
11. **EXT HOLD CAP**
12. **NC**
13. **SUPPLY GND**
14. **S/H CONTROL**

**2 1 14 13**

**3**

**4**

**5**

**6 7 8 9**

**11**

**1**

**.152”**

**NOTE: Chip back must be connected to V-**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .092” X .152” DATE: 8/25/21**

**MFG: HARRIS / INTERSIL THICKNESS .020” P/N: HA0-5320**

**DG 10.1.2**

#### Rev B, 7/1